

Photonic Approach to Optimize Energy Consumption for On-chip Clos Network

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Abstract

To meet energy-efficient performance needs, the computation has positioned to parallel computer architectures, such as chip multiprocessors (CMPs), internally interconnected via networks-on-Chip (NoC) to achieve increasing communication needs. To accomplish scaling execution as center include increment to the hundreds future CMPs, all things considered, will require elite, yet vitality productive interconnects. Silicon Nano photonics is a promising swap for electronic on-chip interconnect for its high data transfer capacity and low inactivity, by the by, earlier methods have required high static force for the laser and warm ring tuning. We propose novel Nano photonic NoC (PNoC) design, upgraded for elite and force effectiveness. This paper makes three essential elements: a novel, Nano photonic engineering which isolates the system into subnets for better productivity; an exclusively photonic, in-band, appropriated discretion plan; and a channel sharing schematic are using the same waveguides and wavelengths for intervention as information transmission. As a result the interconnection can be reduced latency with increased throughput.

Keywords: Low power electronics; Multiprocessor interconnection networks; Nanophotonics; Optical interconnects; Ring resonators

Introduction

The fast hybrid parallel architecture, such as chip multiprocessors (CMPs) have prominent to address power consumption and performance scaling issues in current and future VLSI technologies. Framework on-chip (SoCs) have advanced extensively in term of exhibitions, dependability and incorporation limit [1]. The last favorable position has prompted the development of the quantity of centers or intellectual property (IPs) in the same chip. Lamentably, this essential number of IPs has brought about another issue which is the intra-correspondence between the components of a same chip. To determine this issue another routine network-on-chip (NoCs) has been presented with redesigned techniques and methodologies.

Since an electronic on-chip design had higher power consumption and lower bandwidth management with high latency. To wipe out this issue Photonic Network-on-chip configuration is favored for lessening power utilization and the dormancy with the expanding transmission capacity uses. Since the photonic system on-chip engineering Clos parcel exchanged system is conveyed to exchange extensive data and the circuit exchanged system is just ready to exchange short control message data separately [2].

Other characteristics of these two design methods are the electronic design carries high hardware complexity with area constraints. But in case of photonic design is provided by a small reflection about the devices to capture the signal with low latency [3]. So, a necessary waveguide is used to switch the message signal from photonic to electronic devices as optical to electrical signal transmission respectively and vice versa.

We propose photonic NoCs architecture to address the power consumption and resource overhead for the channel over provisioning, while reducing latency and maintaining high bandwidth in CMPs. This approach is captures in two different ways are a hybrid optical/electrical architecture or crossbar architecture.

The PNoC architecture had three main contributions are as follows. First, instead of conventional, globally distributed optical channels, needs high laser power source with channel sharing arrangement partitioned into number of subnets. Furthermore rather than incorporated design the conveyed discretion plan, dynamic channel booking system is liked to keep up high transfer speed without corrupting throughput, it accomplishes low idleness. Thirdly, same waveguides for same wavelength for exchanging message signal from optical to electrical system configuration is material for permitting best use of force and transmission capacity uses and bringing down force utilization.

Background

PNoCs have prominent as a promising replacement of electronic NoCs for the high bandwidth, low latency, and low power consumption of nanophotonic devices. Figure 1 shows small CMPs with four compute tiles interconnected by a PNoC. Each tile consists of a processor core, private caches, a fraction of the shared last-level cache, and router connecting it to the photonic network [4].

Figure 1 likewise demonstrates the subtle elements of an illustration PNoC, composed as a straightforward, completely associated crossbar interconnecting the four processors. The photonic channel associating the hubs is appeared as being made out of miniaturized scale ring resonators (MRR) incorporated photograph identifiers (PD) (little circles) and silicon waveguides (dark lines interfacing the circles).

Handsets (little triangles) check the limit between the electrical and photonic space.

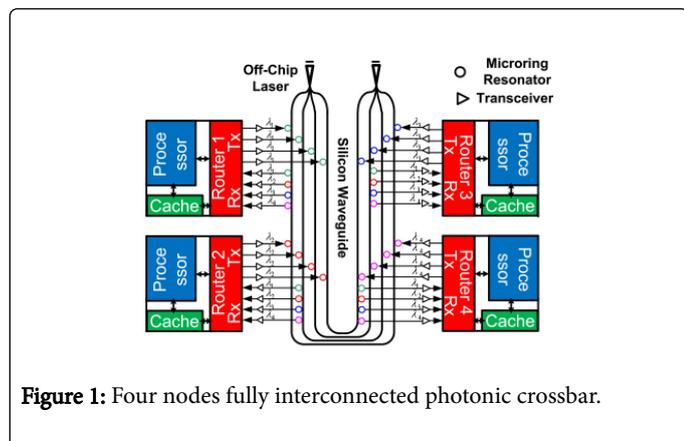


Figure 1: Four nodes fully interconnected photonic crossbar.

While the network shown is non-optimal in terms of scalability, it is sufficient for introducing the components of a simple PNoC.

Overview of Crossbar Functionalities

We describe the various Clos architecture functions;

1. Arbitration scheme
2. Dynamic channel scheduling
3. Switching configurations
4. Deadlock avoidance

Arbitration scheme

Arbitration is a process in which both parties to a dispute ask an independent third party to make a ruling on the matter. The decision of the arbitrator is based on the submissions both parties make and is final and binding.

At a given time a multi wavelength channel consists of many nodes may be in the arbitration schemes to leverage collision detection on data transmission of modulated or detected signal [5]. If one or more senders nodes are modulated any copies of the arbitration flags; one copy of each node keep in subnets fellow ownership for gain control in channel; once a particular sender establishes the communication, it modulates the wavelength in parallel with the data to be transmitted. The mechanism by which the photonic channel is granted by one sender, avoiding data corruption when multiple sender wish to transmit, including dynamic channel scheduling this means sender has conflict resolutions and data transmission credit of mechanism conveyed from sender to receiver.

a) Receiver: Once any collector distinguishes an assertion banner, it will take one of three activities: if the intervention banner is uncorrupted (i.e., the sender banner has a 0 in one and only area showing single-sender) and the inevitable message is bound for this beneficiary, it will empower all its Rx rings for the demonstrated term of the message, catching it. In the event that the discretion banners are uncorrupted, however the collector is not the expected destination, it will detune the greater part of its Rx rings for the demonstrated length of time of the message to permit the beneficiary sole access. At long last, if an impact is recognized, the beneficiary circuit will enter the dynamic channel booking stage.

b) Sender: To send a packet, a node first waits for any on-going messages to complete. Then, it modulates a copy of the arbitration flags to the appropriate arbitration wavelengths for each of the N nodes. The arbitration flags for an example four-node subnet are depicted in Figure 2. The intervention banners are a tarb cycle long header (2 in this case) made up of the destination hub address (D0-D1), a bimodal parcel size marker (Ln) for the two upheld payload lengths (64-bit and 576-piece), and a "1-hot" source address (S0-S3) which serves as a watchman band or impact location instrument: following the subnet is worked synchronously, at whatever time different hubs send covering discretion signals, the "1-hot" precondition is disregarded and all hubs know about the crash. We leverage self-reception of the arbitration flag: right after sending, the node monitors the incoming arbitration flags. If they are uncorrupted, then the sender succeeded arbitrating the channel and the two nodes proceed to the data transmission phase, if the arbitration flags are corrupted.

Dynamic channel scheduling

The static data-to-channel allocation strategy of subnets-enabled DBS-IC works well when network bandwidth adheres to advertised performance. However, in real network deployments the offered bandwidth will vary with changes in channel load, signal strength, and intermittent connectivity [6]. Subsequently, the performance of any static allocation strategy will degrade when available bandwidth diverges from the amount of bandwidth assumed when the static calculation was performed. To assure efficient operation of subnets-enabled DBS-IC, the data-to-channel allocation strategy needs to dynamically adjust in response to changes in network conditions.

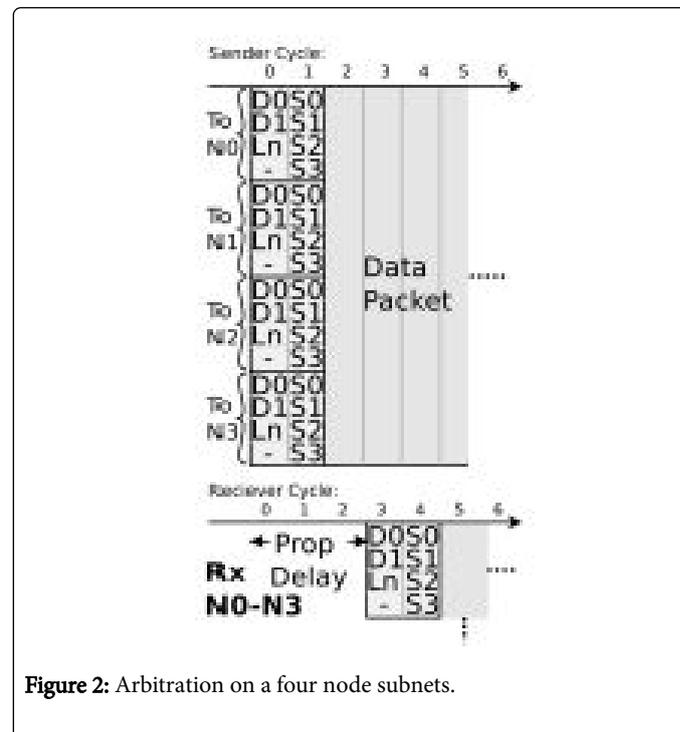


Figure 2: Arbitration on a four node subnets.

To choose a data-to-channel allocation mapping, we use the measured channel available bandwidth and calculate the expected combined throughput of each candidate mapping with respect to cost.

The data-to-channel allocation mapping is chosen as follows. Based on the distribution of throughput combined with cost, the dynamic

mechanism chooses the best data-to-channel allocation mapping as the one with the highest throughput. The dynamic mechanism recurses by finding the next best point located to the left of the previous value.

Upon sensing a conflicting source address, all nodes identify the conflicting senders and a dynamic, fair schedule for channel acquisition is determined using the sender node index and a global cycle count (synchronized at startup): senders transmit in $(n + \text{cycle}) \bmod N$ order [7]. Before sending data in turn, each sender transmits an abbreviated version of the arbitration flags: The destination address and the packet size. All nodes tune in to receive this, immediately followed by the data transmission phase with a single sender and receiver for the duration of the packet. Immediately after the first sender sends its last data flit, next sender repeats this process, keeping the channel occupied until the last sender completes. After the dynamic schedule completes, the channel goes idle and any node may attempt a new arbitration to acquire the channel as previously described.

Switching configurations

The fundamental building block of the photonic network is a broadband photonic switching element (PSE), based on a ring-resonator structure. The switch is, in essence, a waveguide intersection, positioned between two ring resonators (Figure 3). The rings have a specific reverberation recurrence, got from material and basic properties. In the OFF state, when the full recurrence of the rings is not quite the same as the wavelength (or wavelengths) on which the optical information stream is tweaked, the light goes through the waveguide convergence continuous, as though it is a detached waveguide hybrid (Figure 3). When the switch is turned ON, by the injection of electrical current into p-n contacts surrounding the rings, the resonance of the rings shifts such that the transmitted light, now in resonance, is coupled into the rings making a right angle turn (Figure 3), thus creating a switching action [8].

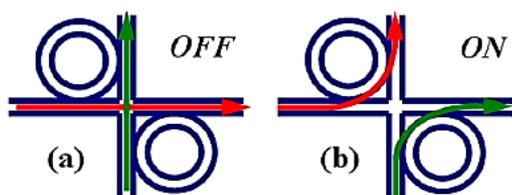


Figure 3: Photonic switching element: (a) OFF state: a passive waveguide crossover. (b) ON state: light is coupled into rings and forced to turn.

Photonic switching elements and modulators based on the fore mentioned effect have been realized in silicon and a switching time of 30 ps has been experimentally demonstrated. Their merit lies mainly in their extremely small footprint, approximately 12 μm ring diameter and their low power consumption: less than 0.5 mW, when ON. When the switches are OFF, they act as passive devices and consume nearly no power.

The PSEs are interconnected by silicon waveguides, carrying the photonic signals, and are organized in groups of four. Each quadruplet,

controlled by an electronic circuit termed an electronic router, forms a 4×4 switch (Figure 4). The 4×4 switches are, therefore, interconnected by the inter-PSE waveguides and by metal lines connecting the electronic routers. Control packets (e.g. path-setup) are received in the electronic router, processed and sent to their next hop, while the PSEs are switched ON and OFF accordingly. Once a packet completes its journey through a sequence of electronic routers, a chain of PSEs is ready to route the optical message. Owing to the small footprint of the PSEs and the simplicity of the electronic router, which only handles small control packets, the 4×4 switch can have a very small area. Based on the size of the micro ring resonator devices, and the minimal logic required to implement the electronic router, we estimate this area at $70 \mu\text{m} \times 70 \mu\text{m}$.

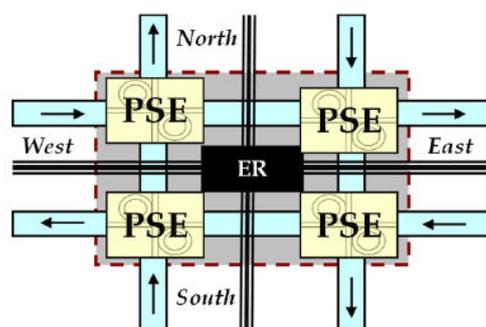


Figure 4: Four photonic switching elements (PSE) controlled by an electronic router (ER).

Deadlock avoidance

A deadlock is a situation in which two or more competing actions are each waiting for the other to finish, and thus neither ever does.

Deadlock is a common problem in multiprocessing systems, parallel computing and distributed systems, where software and hardware locks are used to handle shared resources and implement process synchronization.

In a transactional database, a deadlock happens when two processes each within its own transaction updates two rows of information but in the opposite order. For instance, process A upgrades line 1 then line 2 in the definite time period that procedure B upgrades line 2 then line 1. Process A can't complete the process of upgrading line 2 until procedure B is done, yet procedure B can't get done with upgrading line 1 until procedure A is done. Regardless of the amount of time is permitted to pass, this circumstance will never resolve itself and due to this database administration frameworks will commonly kill the exchange of the procedure that has done minimal measure of work. In an operating system, a deadlock is a situation which occurs when a process or thread enters a waiting state because a resource requested is being held by another waiting process, which in turn is waiting for another resource. If a process is unable to change its state indefinitely because the resources requested by it are being used by another waiting process, then the system is said to be in a deadlock.

Deadlock freedom in the router network, henceforth just network, relies on the consumption assumption: the network accepts and delivers all messages sent by the network interfaces (NIs) as long as they promise to consume all messages from the network when they are

delivered. Routing algorithms that rely on this assumption, which to the best of our knowledge is true for all non-loss routing algorithms currently used in NoCs, are still susceptible to deadlock arising from protocol interactions in the NIs. The IP blocks create message dependencies between buffers in the Nis that, when transferred to the router network, can lead to message dependent deadlocks.

- **Gateway switch:** Injected messages are required to make a turn towards the injection switches. Ejected messages arrive from the ejection message and pass straight through. Therefore, blocking cannot happen
- **Injection switch:** Messages already traveling on the torus network do not turn to the injection paths, so no blocking interactions exist between them and the injected messages
- **Ejection switch:** Messages may arrive only from the torus network and they either turn for ejection or continue straight through. Since no messages arrive from the gateway switch, none of the blocking interactions may happen (Figure 5).

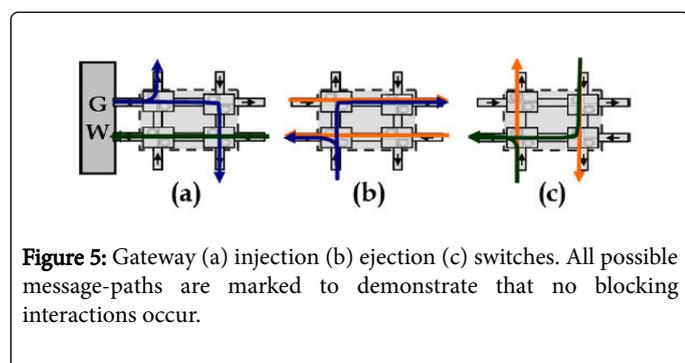


Figure 5: Gateway (a) injection (b) ejection (c) switches. All possible message-paths are marked to demonstrate that no blocking interactions occur.

Proposed system block

The block diagram which explains the basic operation and characteristics of photonic design as shown in the Figure 6. The photonic defines a point-to-point interface between two or more communicating devices such as IP cores and other bus interface modules with the help of optical devices. While transferring data/message signal the sender core act as a master and the receiver core act as slave in order to establish and terminate the communication. A separate control unit is to control access and flows of message/data signaling transfer between the tiles are respect to the scheduling slots.

Since the data signals are arrived from the waveguides with the help of ring resonator to follow the resonance conditions between the circumferences and the number of waveguides traversing in it. Each tile contains λ modulating “TX rings” and λ receiving “RX rings”, where λ is the number of wavelengths multiplexed in the waveguide.

Based on the system architecture Figure 1, the PNoC have several subnets with shorter waveguides of different sizes of 16-nodes CMP system. Here all tiles are interconnected by two diverse subnets, one level and one vertical. In the event that a sender and collector don't live in the same subnet transmission requires a bounce through a middle of the road hub's electrical switch. For this situation, transmission encounters longer defer because of the additional O/E-E/O changes and switch idleness. To remove the overheads of photonic waveguide crossings required by the orthogonal set of horizontal and vertical subnets, the waveguides can be deposited into two layers with orthogonal routing.

Another observation from prior PNoC designs is that channel sharing and arbitration have a large impact on design power efficiency. Efficient utilization of the photonic resources, such as wavelengths and ring resonators, is required to yield the best overall power efficiency. To this end, we leverage the same wavelengths in the waveguide for channel arbitration and parallel data transmission, avoiding the power and hardware overhead due to the separated arbitration channels or networks.

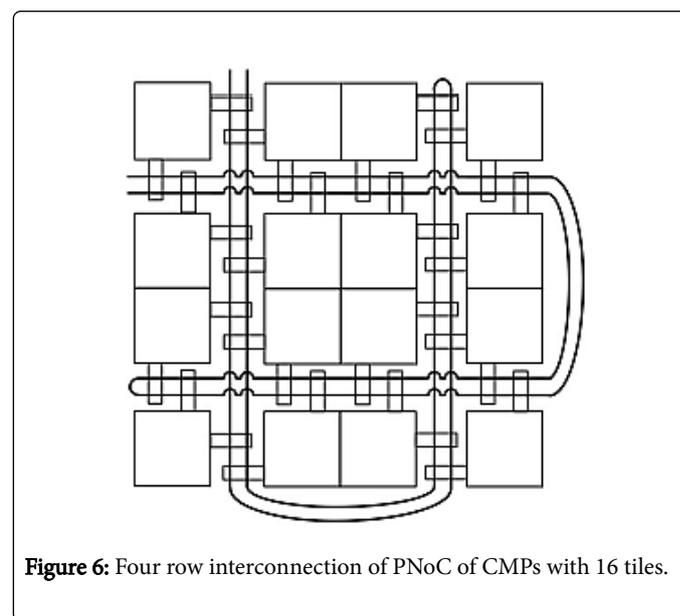


Figure 6: Four row interconnection of PNoC of CMPs with 16 tiles.

Unlike the over-provisioned channels in conventional crossbar architectures, channel utilization in PNoC is improved by multiple tiles sharing a photonic channel.

Results

The design is coded and simulated using different layered configurations. The result analysis of power and latency could be depicted with respect to the system performances (Figures 7 and 8).

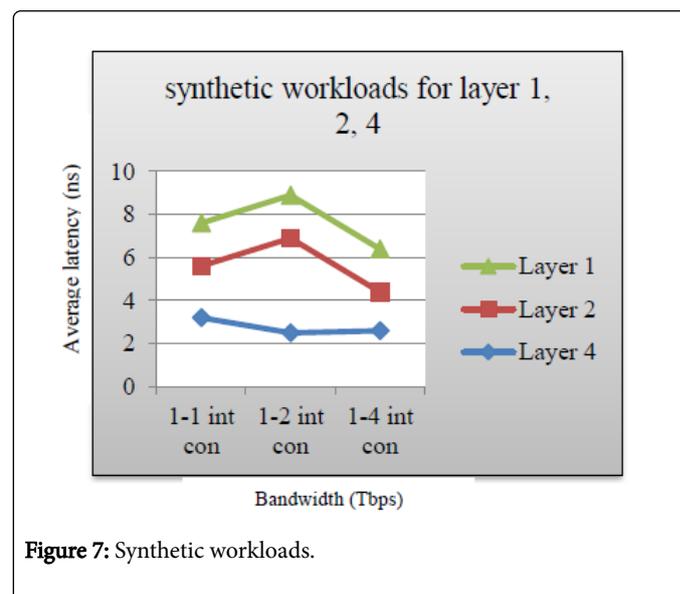


Figure 7: Synthetic workloads.

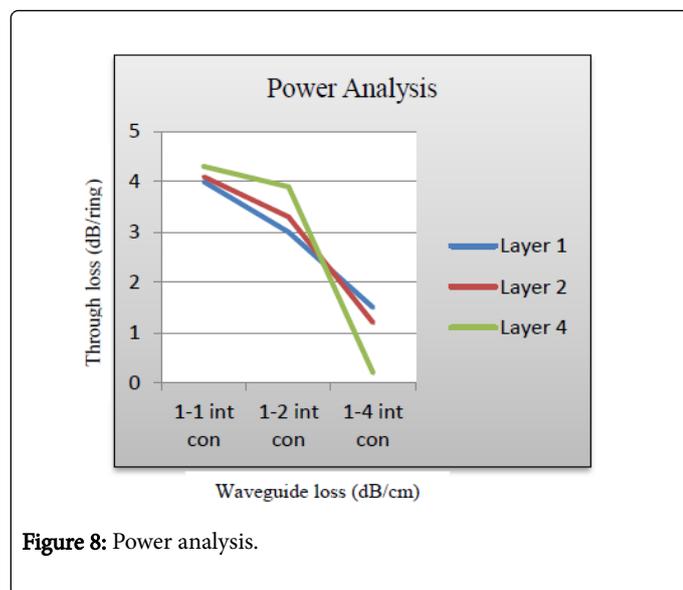


Figure 8: Power analysis.

Conclusion

Cores with PNoCs interfaces and crossbar interconnection enable true modular replacement of electronic design with high bandwidth and low latency of communications. This permitting the framework integrators picks the tiles ideally lessen the force and to work parallel engineering plans. Without lessening the execution of the processors the tile could be reused with no extra time of tile to be reproduced.

Depending up on the continuous applications these interconnection IP centers can be utilized as a part of various on-chip plans proficiently.

References

1. Li C, Browning M, Gratz PV, Palermo S (2014) LumiNOC: A Power-Efficient, High-Performance, Photonic Network-on-Chip. IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems 33: 826 - 838.
2. Deek LB, Almeroth KC, Wittie MP (2008) Exploiting Parallel Networks Using Dynamic Channel scheduling. WICON '08 Proceedings of the 4th Annual International Conference on Wireless Internet 58.
3. Shacham A, Bergman K, Carloni LP (2007) On the Design of a Photonic Network-on-Chip. Proceedings of the First International Symposium on Networks-on-Chip 53-64.
4. Kim H, Ghoshal P, Grot B, Gratz PV, Jiménez DA (2011) Reducing Network-on-Chip Energy Consumption through Spatial Locality Speculation. NOCS.
5. Li C, Bai R, Shafik A, Tabasy EZ (2013) A ring-resonator-based silicon photonics transceiver with bias-based wavelength stabilization and adaptive-power-sensitivity receiver. IEEE International Solid-State Circuits Conference Digest of Technical Papers 124-125.
6. Wang CW, Lai CS, Wu CF, Hwang SA (2008) On-chip interconnection design and sock integration with OCP. IEEE International Symposium VLSI Design, Automation and Test 25 - 28.
7. Naseer Rasool T, Jaffar S, Saheb Basha S (2014) Design and Analysis of Open Core Protocol for the on Chip Bus Using VHDL. International Journal of Science and Research 3: 352-355.
8. Achballah AB, Saoud SB (2013) A survey of network-on-chip tools. International Journal of Advances Computer Science and Applications 4.